What is claimed is:

1. (original) A method for erasing a flash memory, the method comprising:
applying an erase pulse to a block of memory cells;
sequentially reading memory cells of a first sub-block of the block of memory cells;
storing an address of a first memory cell that is determined to be programmed;
applying a second erase pulse to the block of memory cells; and
performing a second sequential reading of the memory cells of the first sub-block starting at the first memory cell address.

2. (original) The method of claim 1 further comprises sequentially reading memory cells of a second sub-block prior to applying the second erase pulse.

3. (original) The method of claim 1 where the address of the first memory cell is stored in an address register corresponding to the first sub-block.

4. (original) The method of claim 1 wherein the address of the first memory cell is loaded into an address counter prior to performing the second sequential reading.

5. (original) A flash memory device comprising:
a memory array comprising a plurality of blocks of addressable memory cells; and
a state machine capable of erasing the flash memory device by applying an erase pulse to a first block of addressable memory cells, sequentially reading memory cells of a first sub-block of the block of addressable memory cells, storing an address of a first memory cell that is determined to be programmed, applying a second erase pulse to the first block of memory cells, and performing a second sequential reading of the memory cells of the first sub-block starting at the first memory cell address.

6. (new) A flash memory system comprising:

a processor for generating memory control signals; and

a flash memory device coupled to the processor, the flash memory device comprising:

a memory array comprising a plurality of blocks of addressable memory cells; and

a state machine that operates in response to the memory control signals, the state machine capable of erasing the flash memory device by applying an erase pulse to a first block of addressable memory cells, sequentially reading memory cells of a first sub-block of the block of addressable memory cells, storing an address of a first memory cell that is determined to be programmed, applying a second erase pulse to the first block of memory cells, and performing a second sequential reading of the memory cells of the first sub-block starting at the first memory cell address.